Sub Code: R2322422 **R23** **Set No. 1**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY-GURUJADA VIZINAGARAM
II B. TECH II SEMESTER SUPPLIMENTRY EXAMINATIONS NOV -2025
DIGITAL LOGIC AND COMPUTER ORGANIZATION
(CSE (AI&DS,AI&ML,AI) AI&DS,AI&ML)

Time: 3 hours **Max. Marks: 70**

The Question paper consists of Part A & Part B.
Part A is compulsory, Answer all questions. Part B Answers any one question from each unit.
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1		PART-A	(20Marks)
	a)	What is meant by an overflow? How can you tell that an overflow has occurred when performing 1's or 2's complement addition**?**	[2]
	b)	Explain 1-bit magnitude comparator using logic diagram?	[2]
	c)	State and prove De-Morgan theorem.	[2]
	d)	Define Pair, Quad, and Octet.	[2]
	e)	What are the classifications of sequential circuits?	[2]
	f)	Explain basic difference between a shift register and counter?	[2]
	g)	List the advantages of Programmable logic devices.	[2]
	h)	Explain the operation of Associative memory.	[2]
	i)	Draw a flow chart that describes the CPU-I/O channel communication.	[2]
	j)	Identify address lines and input–output data lines in each of the below ROM chips? i) 8K ×16 ii) 16M × 32	[2]
		PART-B	(50Marks)
		Question from **Unit - I**	
2	a)	Minimize the function using K-map: F=∑m(1,3,4,6,8,9,12,15) and implement the same using logic gates.	[5]
	b)	A =100010 and B = 010101 are 1's complement numbers. Perform the following operations and indicate whether overflow occurs. i) A + B ii) A – B	[5]
		(OR)	
3	a)	Find the product - of sums expression for f (w, x, y, z) = ∏M (1, 3, 4, 5, 9, 13, 15) using K –map and draw the logic circuit.	[5]
	b)	Explain the design procedure for multiplexers and de-multiplexers and draw the logic diagram of a 4-to-1 line multiplexer with logic gates.	[5]
		Question from **Unit - II**	
4	a)	Design SR Flip Flop using NAND gates and explain its functionality using its truth table?	[5]
	b)	Explain the functionality of Universal shift register shift register with the help of block diagram?	[5]
		(OR)	
5	a)	Explain about the Structure of Bus and types of Bus with a neat diagram?	[5]
	b)	Discuss Von Neumann architecture.	[5]
		Question from **Unit - III**	
6	a)	Explain the following addressing modes and their effective address calculation with suitable examples? i. Immediate ii. Direct iii. Indexed iv. Base with Index and offset	[10]

(OR)

7	a)	Draw the flowchart for Multiplication of positive numbers and steps with an example	[5]
	b)	Explain the techniques in computer arithmetic with example i) Ripple carry adder . ii) Carry look-ahead adder	[5]

Question from **Unit - IV**

8	a)	What is Virtual Memory? Discuss how paging helps in implementing virtual memory.	[5]
	b)	What are differences between RAM & ROM? List out some differences between SRAM & DRAM?	[5]

(OR)

9	a)	What is Cache Memory? Explain in detail its mapping functions.	[5]
	b)	Explain about Memory Hierarchy? Explain about Memory Management Requirements?	[5]

Question from **Unit - V**

10	a)	Describe the use of DMA controllers in a computer system with a neat block diagram.	[5]
	b)	Write about input-output subsystems with neat diagrams?	[5]

(OR)

11	a)	Draw the diagram for the memory module based on its input/output ports, list the main buses then the purpose for each of them.	[5]
	b)	List out few I/O Interfaces and explain about them.	[5]

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